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EXAMINER	
SHERMAN, STEPHEN G	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,395	WASHIO ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-15* is/are allowed.

6)☒ Claim(s) *2-7 and 16-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed 20 November 2007. Claims 2-17 are pending. Claim 1 has been cancelled.

Response to Arguments

2. Applicant's arguments with respect to claims 2-7 and 16-17 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 2-7 and 16-17 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 states the limitation "the first and second signals are signals related to each other which could cause timing discrepancy problems when routed through different wires", which renders the claim indefinite because the word "could" does not allow the examiner to know whether timing discrepancies will happen or not. Therefore, the intentions of the applicant are unclear, and the limitation is indefinite.

For the purposes of examination, the examiner will assume that the applicant intends for there to be timing discrepancies when the signals are routed through different wires.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 2-5, 7 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi et al. (US 6,115,020) in view of Kazunari (JP 11-031747).

Regarding claim 2, Taguchi et al. disclose a display device (Figure 36), comprising:

a scanning signal line driving circuit for driving scanning signal lines (Figure 36, vertical driver circuits 70A and 70B); and

a data signal line driving circuit for driving data signal lines intersecting the scanning signal lines (Figure 36, horizontal driver circuit 71),

at least one of a scanning signal line driving circuit and a data signal line driving circuit being supplied with at least first and second signals (Figure 36 shows that the vertical drive circuit 70B is supplied with a first clock GCKR and a second clock GOER),

the first signal being supplied in parallel to other circuit than the driving circuit supplied with the first and second signals (Figure 36 shows that the clock signal GCKR is applied in parallel through the wiring shown at the top of the figure to the vertical driver circuit 70A.).

the first and second signals are signals related to each other which could cause timing discrepancy problems when routed through different wires (In Figure 36, timing discrepancies will happen between the output enable clock GOER and the clock signal supplied to the vertical driver 70A due to the differing length of wires.).

Taguchi et al. fail to teach the display device further comprising wiring load adjustment section for equalizing wiring load of the second signal which is supplied to the driving circuit, and wiring load of the first signal which is supplied in parallel to the driving circuit and the other circuit.

Kazunari discloses of a display device comprising a wiring load adjustment section for equaling the wiring load of two signals in which the wirings are of different length (Figure 4 and paragraph [0030] explain that wiring 316 has a partial wiring

connected to it, which has a capacitance of 316-A, allowing for the load capacitances of the wirings to be equal.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the teachings of Kazunari with the teachings of Taguchi et al. in order to reduce a difference in delay of the clocks.

Regarding claim 3, please refer to the rejection of claim 1.

Regarding claim 4, Taguchi et al. and Kazunari disclose the display device as set forth in claim 2.

Kubota et al. also discloses wherein the first signal is supplied to the driving circuit and the other circuit from a common input terminal and through a common signal line (Figure 36 shows that the signal GCKR is supplied to the two driving circuits 70A and 70B from a common input GCKR and is supplied to both circuits using the same signal line.).

Regarding claim 5, Taguchi et al. and Kazunari disclose the display device as set forth in claim 2.

Taguchi et al. also discloses wherein first and second signals are clock signals of plural systems, respectively (Figure 36 shows signals GOER and GCKR.).

Regarding claim 7, Taguchi et al. and Kazunari disclose the display device as set forth in claim 2.

Kazunari also discloses wherein the wiring load adjustment section adjusts time constants of the respective wirings of the first and second signals (Figure 4 and paragraph [0030]. The examiner interprets that since the partial wiring is added in order to equalize a delay of the different clock signals, then the time constants are being adjusted.).

Regarding claim 17, Taguchi et al. and Kazunari disclose the display device as set forth in claim 2.

Taguchi et al. and Kazunari fail to teach wherein the wiring load adjustment section is provided in the scanning signal line driving circuit, however, to place the wiring load adjustment section in a specific location of the circuit does not provide any specific benefit and thus would have been a matter of design choice.

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi et al. (US 6,115,020) in view of Kazunari (JP 11-031747) and further in view of Kim (US 5,808,596).

Regarding claim 6, Taguchi et al. and Kazunari disclose the display device as set forth in claim 2.

Taguchi et al. and Kazunari fail to teach wherein the signals are digital image signals constituted of a plurality of bits, and are divided into at least two bit groups.

Kim discloses wherein signals are digital image signals constituted of a plurality of bits, and are divided into at least two bit groups (Figure 2 and column 3, lines 40-57 explain that the signals (b) and (c) are pixel data, i.e. image signals, where it is well know that pixel data can be in digital form constituted of a plurality of bits being divided into at least two bit groups.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the idea of compensating for delay of image signals as taught by Kim with the display device taught by the combination of Taguchi et al. and Kazunari in order to create a high resolution liquid crystal display which does not require excessive increases in clock frequency in order to increase resolution.

9. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi et al. (US 6,115,020) in view of Kazunari (JP 11-031747) and further in view of Kubota et al. (US 2002/0075249).

Regarding claim 16, Taguchi et al. and Kazunari disclose the display device as set forth in claim 2.

Taguchi et al. and Kazunari fail to teach wherein the other circuit is a pre-charging circuit for carrying out pre-charging of the data signal lines.

Kubota et al. disclose a display device having a data driver and a pre-charging circuit which receive clock signals with wiring of different lengths (Paragraph [0620] and Figure 26).

Therefore, it would have been obvious to "one of ordinary skill" in the art at time the invention was made to use the wiring adjustment display device method taught by the combination of Taguchi et al. and Kazunari with the data driver pre-charging circuit of Kubota et al. in order to compensate for the clock delays between the drivers in the device of Kubota et al.

Allowable Subject Matter

10. Claims 8-15 are allowed.

11. The following is an examiner's statement of reasons for allowance:

Regarding claim 8, the main reason for indicating allowable subject matter is that the closest prior references (APA, Kazunari and Kim) fail to teach that the wiring load adjustment section uses the liquid crystal layer as a dielectric substance, and is constituted of dummy wiring connected to the wiring of the second signal which is supplied to the driving circuit and a liquid crystal layer on the dummy wiring, and the counter electrode.

***Regarding claim* 12**, the main reason for indicating allowable subject matter is that the closest prior references (APA, Kazunari and Kim) fail to teach that the wirinq load adjustment section uses the interlayer insulation film as a dielectric substance, and is constituted of dummy wiring connected to the wiring of the second signal supplied to the driving circuit, the interlayer insulation film, and the conductive film.

Regarding claim 14, the main reason for indicating allowable subject matter is that the closest prior references (APA, Kazunari and Kim) fail to teach that the wiring load adjustment section uses layers for constituting a gate insulation film of a thin film transistor as a dielectric substance, and is constituted of dummy wiring connected to the wiring of the second signal supplied to the driving circuit, and layers for constituting a gate insulation film and a semiconductor layer of a thin film transistor stacked on the dummy wiring.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

31 December 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER